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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,388	03/23/2004	Keiji Hosotani	250922US2S	2356
22850	7590	08/23/2005		
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				
			EXAMINER PIZARRO CRESPO, MARCOS D	
			ART UNIT 2814	PAPER NUMBER

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/806,388

Applicant(s)

HOSOTANI, KEIJI

Examiner

Marcos D. Pizarro-Crespo

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 9-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/23/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Application/Control Number: 10/806,388 (Non-Final Rejection)
Art Unit: 2814

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Attorney's Docket Number: 250922US2s

Filing Date: 3/23/2004

Claimed Foreign Priority Dates: 3/18/2004 (JP 2004-077814)
7/10/1003 (JP 2003-195187)

Applicant(s): Hosotani

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the election filed on 7/5/2005.

Election/Restrictions

1. Applicant's election without traverse of claims 1-8 in the reply filed on 7/5/2005 is acknowledged. Claims 9-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang (US 6864551) in view of Wallace (US 6143634).

6. Regarding claim 1, Tsang (see, e.g., fig. 5A) shows most aspects of the instant invention including a magnetic random access memory comprising:

- ✓ A substrate **202**
- ✓ A transistor **210** having:
 - A gate electrode **215** formed on the substrate **202** via a gate insulating film
 - Diffusion layers **212/213** formed in the substrate **202**
- ✓ A first insulating film formed on the substrate **202** and the transistor **210**
- ✓ A multilayered interconnection **219** formed in the first insulating film
- ✓ A magneto-resistive element **11** formed above the first insulating film

Tsang, however, fails to show that the substrate is made of silicon and that silicon-deuterium bonds terminate some of the dangling bonds in the substrate. Wallace, on the other hand, teaches that hydrogen passivating of the dangling bonds in a substrate improves device function (see, e.g., col.1/ll.10-15). Deuterium, an isotope of hydrogen, may also be used for passivating and being more stable than regular hydrogen it improves hot-channel-carrier lifetime (see, e.g., Wallace/col.1/ll.15-20).

Wallace also forms (see, e.g., fig. 2) the transistor on a silicon substrate **200** via a gate-insulating layer **210**.

It would have been obvious at the time of the invention to one of ordinary skill in the art to passivate the dangling bonds of Tsang's substrate with deuterium, as suggested by Wallace, to improve the hot-channel-carrier lifetime of the device.

7. Regarding claim 7, Wallace shows that the magneto-resistive element **11** is electrically connected to the transistor **210** through part of the multilayered interconnection **219**, and the transistor **210** is a data read switching element (see, e.g., col.2/ll.8-17).

8. Regarding claim 8, Tsang shows the transistor is a transistor of a CMOS circuit (see, e.g., col.7/ll.53).

9. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang/Wallace in view of Van de Walle.

10. Regarding claims 2-6, Tsang/Wallace show most aspects of the instant invention (see, e.g., paragraphs 6-8 above) but fail to specify that the deuterium exist at least partially in an interface portion between the gate insulating film and the substrate under the gate electrode, in junction portions of the diffusion layers, in a channel portion, in the first insulating film, in the gate electrode, in the gate insulating film, and in the second insulating film. Wallace, on the other hand, teaches to follow each one of the fabrication steps of the device with a deuterium anneal (see, e.g., fig. 1). Although not specified by Wallace, this implies that deuterium will be present everywhere throughout the device.

See, e.g., Van de Walle/pp.1780/col.2/ll.30-35, who teaches that hydrogen is omnipresent during semiconductor device processing.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that deuterium would exist at least partially in an interface portion between the gate insulating film and the substrate under the gate electrode, in junction portions of the diffusion layers, in a channel portion, in the first insulating film, in the gate electrode, in the gate insulating film, and in the second insulating film of Tsang/Wallace since hydrogen is omnipresent during semiconductor device processing, as taught by Van de Walle.

11. Regarding claim 6, Wallace shows (see, e.g., fig. 2) a second insulating film **280** formed on the silicon substrate **200**, including upper surfaces of the diffusion layers **270**, and upper and side surfaces of the gate electrode **220**.

Conclusion

12. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

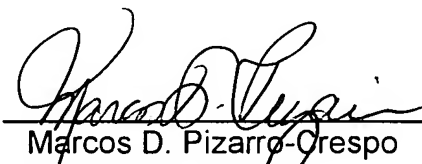
13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through

Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

14. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

15. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/421-427, 288-412	8/19/2005
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	8/19/2005


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